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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
RUTLAND WALLIS, MICHAEL	
ART UNIT	PAPER NUMBER
2836	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/822,856	JACOBS ET AL.	
	Examiner	Art Unit	
	Michael Rutland-Wallis	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40 and 47-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-40 and 47-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/12/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 1-40 and 47-54 in the reply filed on 03/26/2007 is acknowledged.

Drawings

New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because Applicant has only submitted hand drawn figures with labeling and numberings.

Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Objections

Claim 33 recites the limitation "the housing" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 47 are rejected under 35 U.S.C. 102(b) as being anticipated by Vinciarelli (U.S. Pat. No. 6,975,098)

With respect to claim 1 Vinciarelli teaches a power supply system (Fig. 7 for example or Fig. 2) comprising: a package housing (PCB subassemblies items 42); a first module (66A), located within the package housing (42), the first module comprising at least one first power conversion switch (contained within the DC-DC converters items 48 and/or switching regulators 65 and/or other voltage transformation module seen detailed in Fig. 9) structured to perform power conversion switching to facilitate conversion of a first power input signal (Vf or Vin connected to the converter input) into a first power output signal (V1); and a second module (66B), located within the package housing (42), the second module comprising at least one second power conversion switch (contained within the DC-DC converters items 48 and/or switching regulators 65) structured to perform power conversion switching to facilitate conversion of a second

power input signal (voltage input into the second power conversion module) into a second power output signal (V2).

With respect to claim 47 Vinciarelli teaches a method of supplying power in a computer, the method comprising the following steps: providing a switching power supply system (switching system comprised on converters and switching regulators) for outputting a plurality of power output signals (seen in Fig. 7 for example), the system comprising: a package housing (PCB subassemblies items 42); and a plurality of power conversion switches (contained within the DC-DC converters items 48 and/or switching regulators 65) located within the package housing, the power conversion switches for performing the power conversion switching necessary to convert at least one power input signal (Vf) into the plurality of power output signals; and controlling the operation of the power conversion switches by power management commands (see switch controller 130 generating control signal controlling the switching within the converters) in order to selectively and individually control the plurality of power output signals.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-7, 9-22 and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vinciarelli (U.S. Pat. No. 6,975,098)

With respect to claims 2-4 Vinciarelli teaches a plurality of modules (see 42e) may be mounted on the package however is not directed toward specific output power conversion ratios (e.g. one third or one fourth power conversion) rather Vinciarelli simply notes the converter should convert the output voltage to that which required by the load citing several typical voltages in col. 2 such as: 2v, 5v and 12v. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Vinciarelli to use the third, fourth and fifth modules to utilize a one third, one fourth and one fifth power conversion respectively in order to produce a plurality of voltages that may be used by different load found in a computer system.

With respect to claims 5 and 6 Vinciarelli teaches all power conversion switches required for respectively converting the first and second power input signals into the first and second power output signals are located within the package housing.

With respect to claim 7 Vinciarelli teaches the first power input signal is a dc signal; the first power output signal is a dc signal; the second power input signal is a dc signal; and the second power output signal is a dc signal.

With respect to claims 9 and 10 Vinciarelli teaches the at least one first and second power conversion switch is structured to perform efficient power conversion. Vinciarelli does not describe the conversion as ultra high efficiency. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify to

Vinciarelli use more efficient switches if in fact the switches are not already considered ultra efficient in order to reduce excess heat.

With respect to claim 11 Vinciarelli teaches the at least one first power conversion switch is structured to perform at an efficient power conversion which one may construe a high or a low efficiency.

With respect to claim 12 Vinciarelli teaches the first module comprises at least two first power conversion switches (items 58 and 60 for example) structured to perform power conversion switching to facilitate conversion of the first power input signal into the first power output signal; and the second module comprises at least two second power conversion switches structured to perform power conversion switching to facilitate conversion of the second power input signal into the second power output signal.

With respect to claims 13 and 14 Vinciarelli teaches the system is configured to provide power to diverse electrical components in an electronic system which one skilled in the art may construe a high or a low power.

With respect to claim 15 and 16 Vinciarelli teaches the first and second power conversion switches are operable so that the power output signal has an adjustable voltage output in the range of about +0.5 volts to +2.0 (col. 2 line 20-25) volts. Vinciarelli does not specifically citing the powering of the CPU with specifically 2 volts however it would have been obvious to one of ordinary skill in the art at the time of the invention to supply such a voltage to the core of the CPU in order for the CPU to receive the proper input voltage to perform properly.

With respect to claim 17-21 Vinciarelli teaches the output voltages are typical output voltages known to one skilled in the art citing several typical voltages in col. 2 such as: 2v, 5v and 12v. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Vinciarelli to output any power conversion with a typical range of devices found in computing devices.

With respect to claim 22 Vinciarelli teaches the system comprises a bridge (i.e. is connected between the supply and load) between at least one power supply and a central processing unit (not shown).

With respect to claim 25 Vinciarelli teaches the a control logic (120) block, located within the package housing, the control logic block being structured and located to at least partially control the operation of the at least one first power conversion switch (s1) and the at least one second power conversion switch (s2).

With respect to claim 26 Vinciarelli teaches a first switch driver (130) for controlling the position of the at least one first power conversion switch (s1); a second switch driver for controlling the position of the at least one second power conversion switch (s2); a control input/output port (switch control ports), located within the package housing, the control input/output port being structured and located to receive at least one communication signal from outside of the package housing, wherein: a mode of the first and second power conversion switches is determined by the communication signal; and the operation of the first and second switch drivers is controlled by the control logic block based at least in part by the mode.

With respect to claim 27 Vinciarelli teaches a control input/output port, located within the package housing, the control input/output port being structured and located to receive at least one communication signal from outside of the package housing.

Claims 8 and 37-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vinciarelli (U.S. Pat. No. 6,975,098) in view of Kim et al. (U.S. Pat. No. 5,955,797)

With respect to claim 8 Vinciarelli teaches the first power input signal is a dc signal; the second power input signal is a dc signal; and the second power output signal is a dc signal. Vinciarelli does not teach output of an AC signal. Kim teaches the use of a plurality of conversion modules and also teaches the use of an inverter (item 134) to provide AC power to a back light system (item 136) of a display. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Vinciarelli to include the use of such an output in order to provide an output capable of supplying a display or other load requiring an AC voltage output.

With respect to claim 37 Vinciarelli teaches the system on claim 1 however does not teach the further inclusion of a battery and detailed charging outputs. Kim teaches a first battery (battery within battery pack item 20); a first battery-charging output (item 100), the first battery charging output having an adjustable voltage and current suitable for charging the first battery; a first battery current path structured and located to electrically connect the first battery and the first battery-charging output so that the first battery can be charged by electrical power from the first battery-charging output. It would have been obvious to one of ordinary skill in the art at the time of the invention to

battery pack and charging output located on the package of the Vinciarelli in order to provide regulated power to charge the batteries of a laptop computer.

With respect to claim 38 Kim teaches the use of a communication and control channel to charging circuit see output of item 120 connected to the charging circuit. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Vinciarelli to include use a serial communication interface to control the charging current to the battery.

With respect to claim 39 Kim teaches a battery pack known to contain plural batteries however depicts only one output to the charge the battery. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kim to duplicate the battery and charger to include a second battery and battery charging unit in order to have a redundant battery system and charging line.

With respect to claim 40 Vinciarelli teaches the use of voltage transformers and output lines associated with the transformers, however is silent on the particular loads connected thereto. Kim teaches the use of an inverter to transformer the output power to power a backlight for a display. It would have been obvious to one of ordinary skill in the art at the time of the invention to include such an AC output line a on the package of the Vinciarelli in order to provide regulated power to provide a regulated voltage to a display of a computing system.

Claims 28-36 and 48-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vinciarelli (U.S. Pat. No. 6,975,098) in view of Wright (U.S. Pat. No. 6,541,879)

With respect to claims 28, 29 and 48 Vinciarelli teaches does not detail the sub steps of sending and receiving power management signals through a USB. Wright teaches plural modules (110) mounted on a circuit connected to a USB management controller to send and receiving power management controls among other things. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Vinciarelli to include the connection of such a control interface in order to supply multiple devices connected to a USB hub.

With respect to claims 31 and 49 Vinciarelli teaches does not detail the sub steps of sending and receiving power management signals through a embedded controller. Wright teaches plural modules (110) mounted on a circuit connected to an embedded management controller to send and receiving power management controls among other things. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Vinciarelli to include the connection of such a control interface in order to supply multiple devices connected to a hub to increase power density.

With respect to claims 30 and 50 Vinciarelli teaches the use of a controller however does not teach the use of an I2C protocol. Wright teaches the power management commands are sent from the embedded controller to the control input/output port through serial bus. I2C is a well know protocol used to peripherals to a motherboard or the like and would have been obvious to one of ordinary skill in the art at the time of invention to utilize an I2C protocol in the command transmission in order to communicate with devices to reduce jitters in the connection.

With respect to claims 32 and 51 Vinciarelli teaches the use of a controller however does not teach the use of an I2C protocol. Wright teaches the power management commands are sent from the embedded controller to the control input/output port through serial bus. SMbus is a well know protocol used to peripherals to a motherboard or the like and would have been obvious to one of ordinary skill in the art at the time of invention to utilize an SMbus protocol in the command transmission in order to communicate with devices to reduce jitters in the connection.

With respect to claim 33 Vinciarelli teaches the system for a computing system and an on/off control block (130), located within the housing, the on/off control block being structured and located to initiate a power up process and supply power to the load. Vinciarelli does disclose the use of computer system. Wright teaches a control block and enable circuitry connected thereto. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Vinciarelli to use such a control block to turn the power on and off when the power is not needed.

With respect to claim 34 Wright teaches the computer comprises an on/off switch; and the on/off control block comprises an on/off port for interfacing with the on/off switch.

With respect to claim 35 Wright teaches the on/off port is designed for ultra-low power consumption when the computer is in a power-off condition (no power is used).

With respect to claim 36 Vinciarelli teaches a controller may be embedded wherein Vinciarelli as modified by Wright teaches the on/off control block comprises power-up module structured and located to power up the controller.

Claims 23-24 and 52-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vinciarelli (U.S. Pat. No. 6,975,098) in view of Klughart (U.S. Pat. No. 6,396,137)

With respect to claim 23 Vinciarelli teaches the system of claim 1 however does not teach the detailed manufacturing technique such a flip chip style die. Klughart teaches the use of a flip chip style die (Fig 26). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Vinciarelli to use a flip chip style die in order to reduce manufacturing costs.

With respect to claim 24 Vinciarelli teaches the mounting of the converters to subassemblies however does not illustrate the configuration at the die architecture level. Klughart teaches the semiconductor die level in Fig 26 for mounting a converter. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Vinciarelli to use at least one semiconductor die in the first and second modules if in fact such is not already present in order to simply fabricate the converter.

With respect to claims 52-54 Vinciarelli teaches a switching power supply comprising: a package housing (PCB subassemblies items 42) having an interior (side facing out) and having an exterior surface (side facing in); an integrated circuit chip (each module configured on the subassembly) packaged within the packaged housing (42), the integrated chip including at least one power conversion switch (contained within the DC-DC converters items 48 and/or switching regulators 65 and/or other voltage transformation module seen detailed in Fig. 9) for converting a first power input signal (Vf) into a first power output signal (Vout). Vinciarelli also teaches the use of an

output capacitor (for example 56) connected across the output terminals to be connected to the load (120). Vinciarelli does not describe the capacitor as external or that it is mounted to the surface of the package. Klughart teaches the mounting of capacitor externally (see Fig. 26). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Vinciarelli to mount the capacitor to the surface of the package in order to use of a large storage capacitor to provide a smooth voltage output to the load without using excessive space.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Rutland-Wallis whose telephone number is 571-272-5921. The examiner can normally be reached on Monday-Thursday 7:30AM-6:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 571-272-2084. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MRW

5/29/07

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